

IMPORTANT DATES AND TIME

- ◆ Start Date of Registration: 12-05-2026
 - ◆ Last Date of Registration: 01-07-2026
 - ◆ Per Day Timings: 02.00 pm – 06.00 pm
 - ◆ Course Hours: 40 Hrs
- (Including Theory, Hands-on & Evaluation)

Registration Fees

Rs. 500/- (Inclusive of GST)

Mode of Payment Online Only

Details for Online Transfer

Beneficiary Name	PDPM IIITDM Jabalpur
Bank Name	INDIAN BANK
A/C No.	50018692852
IFSC Code	IDIB000M694
UPI ID:	iiitdmj@indianbk



An Initiative of Ministry of Electronics & Information Technology (MeitY), Government of India

Electronics & ICT Academy
IIT Guwahati, IIT Kanpur, MNIT Jaipur, IIT Roorkee & IIITDM Jabalpur




Presents

Two - Weeks Joint Faculty Development Programme on

VLSI 102: Digital CMOS Circuit Design

06 July to 17 July 2026

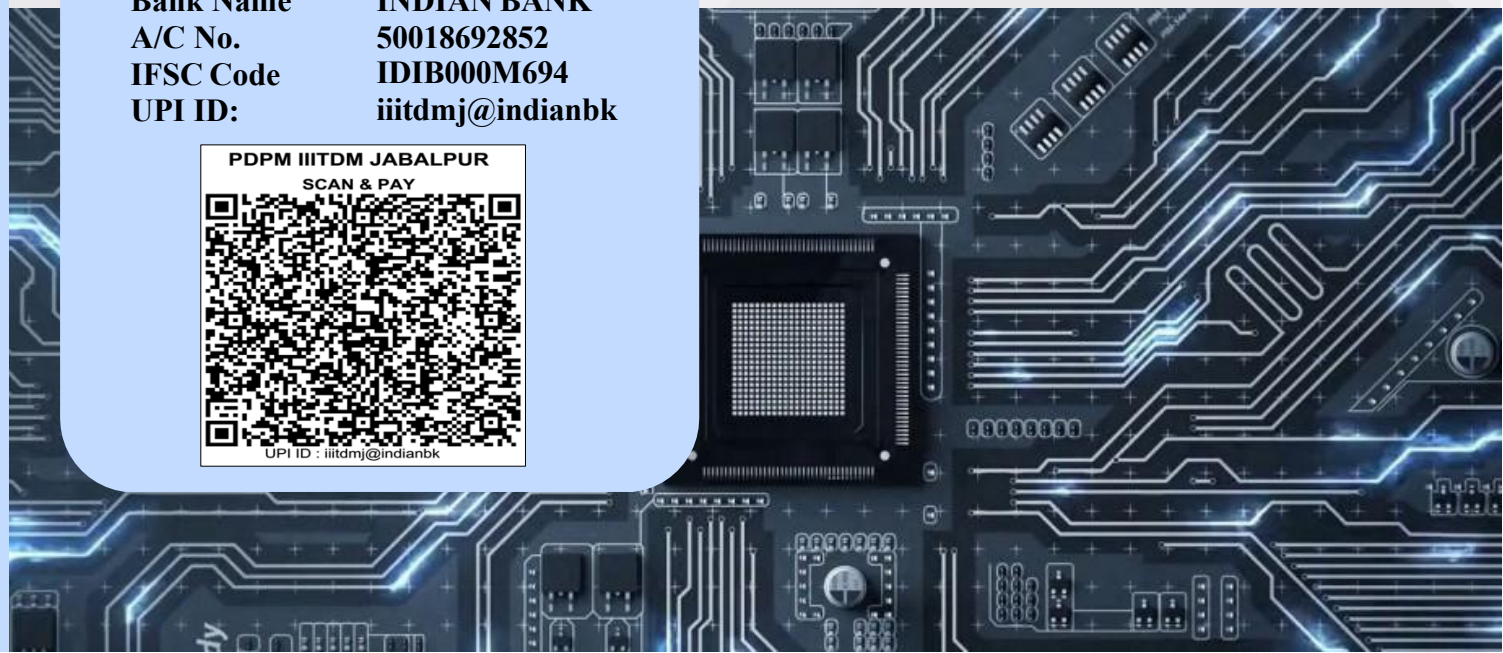
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 Electronics and ICT Academy Phase-II- IIITDM Jabalpur

 **Indian Institute of Information Technology Design & Manufacturing Jabalpur**



COURSE OBJECTIVES

This two weeks Programme is designed:

1. To introduce participants to the fundamentals of MOS transistor operation and CMOS fabrication technology.
2. To develop understanding of CMOS logic families, inverter characteristics, and digital circuit behavior.
3. To introduce concepts of layout design, design rules, parasitic effects, and physical verification techniques.
4. To train participants in transistor-level circuit design and simulation methodologies using industry-relevant EDA tools.

COURSE OUTCOMES

After successful completion of the course, participants will be able to:

1. Understand the operating principles and characteristics of MOS transistors and CMOS fabrication technology.
2. Analyze and design basic and complex CMOS logic circuits using transistor-level design methodologies.
3. Utilize EDA tools for schematic entry, circuit simulation, verification, and analysis of CMOS circuits.
4. Develop CMOS layouts while adhering to design rules and understand the impact of parasitic effects on circuit performance.
5. Evaluate propagation delay, power dissipation, noise margins, and reliability aspects of CMOS digital circuits.

Principal Coordinators

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ASSIGNMENT AND HANDS-ON

There will be total two MCQ assignments in the entire programme which will be conducted through Google Forms. Hands-on sessions will be followed by the theory lectures.



Mode of Delivery: Online through Webex

HOW TO REGISTER

Online: The participants may log on to the E&ICT Academy, IIT Guwahati website: <https://forms.gle/sPFsz1pfF3qsZ7Vj8>

PLEASE NOTE THAT



- Registration fees include evaluation and participation certificate.
- Participants have to submit UTR No. as the proof of payment while registering for the Faculty Development Programme.
- Registration Fees is Refundable if the registration cancellation request is submitted before the last date of registration.

